CIRCUIT AND METHOD FOR ESD PROTECTION

FIELD OF THE INVENTION

[0001] The present invention relates to a circuit and a method for semiconductor integrated circuits. More particularly, the present invention relates to a circuit and a method for electrostatic damage (ESD) protection.

DESCRIPTION OF THE RELATED ART

[0002] Because of high level integration of semiconductor integrated circuits, product reliabilities are important for the integrated circuits, e.g. vulnerability to electrostatic damage (ESD). An ESD pulse may occur when pins and/or input/output bond pads of the integrated circuits are charged with a high voltage or from current resulting from a body or material that is statically charged. Usually the voltage charge is more than 100V for a short period time, e.g. about 10 to several hundred nanoseconds (ns). Internal devices of the integrated circuits typically cannot suffer the abnormal voltage pulse resulting from the short but sharp voltage or current pulse, and are often easily destroyed. Therefore, ESD protection circuits are designed and connected to pads and the internal integrated circuits to provide an additional current path for bypassing the voltage or current pulse to a safe connection point.

[0003] Usually, an ESD protection circuit is triggered under high field strengths in conjunction with PNP and NPN bipolar transistors, which together form a silicon controlled rectifier (SCR). However, the triggering voltage of the ESD protection circuit must be low enough to prevent gate oxide breakdown of the MOS devices within an internal circuit. More specially, it is difficult to design a low capacitance ESD (LCESD) protection circuit while protecting the thin gate oxide from an ESD pulse because additional devices designed in a LCESD protection circuit will increase the capacitance of the circuit.

[0004] **Fig. 1** schematically illustrates a conventional LCESD protection circuit. Input/output (I/O) pad 110 is coupled to a first connector of LCESD protection circuit 120. A second connector of LCESD protection circuit 120 is coupled to a V_{SS} terminal, e.g. ground. I/O pad 110 is also connected to functional circuit 130 which may further include an inverter or other buffer circuit, e.g NMOS transistors 131 and 132, and internal circuit 133. The source terminal of NMOS transistor 132 is coupled to a V_{SS} terminal.

[0005] When an ESD pulse is coupled to I/O pad 110, LCESD protection circuit 120 will be triggered to protect functional circuit 130. However, the thin gate oxide layers of NMOS transistors 131 and 132 may be broken down before LCESD protection circuit 120 is triggered. Therefore, LCESD protection circuit 120 cannot efficiently protect functional circuit 130 from damage resulting from the ESD pulse.

[0006] Therefore, it is desirable to provide a circuit and a method to resolve the issues within the semiconductor integrated circuits mentioned above.

BRIEF DESCRIPTION OF THE DRAWINGS

[0007] **Fig. 1** schematically illustrates an ESD protection circuit in accordance with a prior art.

[0008] **Fig. 2** schematically illustrates an exemplary embodiment of a circuit for ESD protection in accordance with the present invention.

DESCRIPTION OF A PREFERRED EMBODIMENT

[0009] **Fig. 2** illustrates a preferred embodiment of a circuit for ESD protection. The circuit comprises pad 210, functional circuit 250, ESD protection circuit 220 operatively coupled to pad 210 and functional circuit 250, first resistive device 230 coupled to pad 210 and functional

circuit 250, and active device 240 operatively coupled to first resistive device 230 and ESD protection circuit 220.

[0010] Pad 210 may be coupled to a first connector of ESD protection circuit 220 and to resistive device 230. Pad 210 can be, for example, an input/output power pad or an input/output signal pad.

[0011] ESD protection circuit 220 can be, for example, a traditional ESD protection circuit or low capacitance ESD (LCESD) protection circuit. A second connector of ESD protection circuit 220 may be coupled to a V_{SS} terminal and V_{SS} may further be operatively coupled to ground.

[0012] Resistive device 230 may be connected intermediate pad 210 and functional circuit 250, e.g. to gates of NMOS inverter transistors 251 and 252. Resistive device 230 may be used to effect a voltage drop between pad 210 and functional circuit 250 and can be a resistor, a diode, a transistor, or the like, or a combination thereof. In the embodiment illustrated in **Fig. 2**, resistive device 230 is a resistor with an impedance of from about 1 ohm to about 100 ohms.

[0013] Parasitic capacitance of resistive device 230 should not be so high that resistance-capacitance (RC) delay of the circuit will substantially degrade the performance of the overall circuit. Accordingly, parasitic capacitance of resistive device 230 may be adjusted to achieve the desired voltage drop between pad 210 and functional circuit 250 while not disturbing the performance of the circuit.

[0014] Resistive device 230 may be physically separated from ESD protection circuit 220. In other embodiments, resistive device 230 may be embedded in ESD protection circuit 220, e.g. depending on the size of the ESD protection circuit 220 or the ESD protection

performance of the circuit. For example, separating device 230 from ESD protection circuit 220 may improve the performance of ESD protection.

[0015] Functional circuit 250 comprises internal circuit 253 and may further comprise a buffer circuit, e.g. NMOS inverter transistors 251 and 252, disposed intermediate pad 210 and internal circuit 253. In this embodiment, the source terminal of NMOS transistor 251 may be coupled to a voltage terminal, e.g. a V_{DD} terminal. Internal circuit 253 may comprise numerous components, e.g. active and/or passive circuits (not shown in the figures) such as an input buffer, an output buffer, a pre-driver circuit, a level-shift circuit, an amplifier, a power supply, or any other circuit that provides functionality for the operation of internal circuit 253.

[0016] When an ESD pulse is present at pad 210, the ESD pulse will trigger ESD protection circuit 220 into an "on" state. ESD protection circuit 220 then redirects the ESD pulse to the V_{SS} terminal. Additionally, as resistive device 230 may also effect a voltage drop between pad 210 and functional circuit 250, the exemplary circuit illustrated in **Fig. 2** may be used to protect thin gate oxide layers of NMOS transistors 251 and 252 from ESD damage.

[0017] Although the present invention has been described in terms of exemplary embodiments, it is not limited thereto. Rather, the appended claims should be constructed broadly to include other variants and embodiments of the invention which may be made by those skilled in the field of this art without departing from the scope and range of equivalents of the invention.